STORAGE STRUCTURE WITH CLEAVED LAYER

Background of the Invention

The demand for semiconductor devices has increased dramatically over the years. Many frequently used electronic devices are made possible because of developments in semiconductor devices. As such devices become smaller, more sophisticated, and less expensive, the marketplace demands increasingly higher circuit densities, increased performance, and lower cost.

Increasing the density of semiconductor devices has been accomplished by reducing associated component area. Photolithography is nearing X-ray energy levels, however, and is encountering limits in further size reductions. Three-dimensional semiconductor-based structures have provided additional opportunities to increase density, but error probabilities are multiplied as the number of stacked layers increases, and statistics of yield quickly become unsatisfactory.

Crystal-based semiconductor devices generally provide better results than other devices, because regular arrays of atoms provide better electron movement than disordered arrays. At the same time, oxides are needed to keep electrons out of certain areas. Crystals cannot easily be stacked on top of amorphous or non-crystalline oxides, because crystal growth on top of a disordered substrate impedes proper registration of new atoms across the surface and often results in polycrystalline material. Additionally, once a device and a layer have been created, it is generally deleterious to subject them to further thermal input, as is often needed when a next layer is being formed. These and other challenges increase the difficulties and costs associated with stacked devices.

Summary of the Invention

Apparatus and method for making a multi-layered storage structure includes forming a device layer on a single-crystal wafer, cleaving the device layer from the wafer, repeating the forming and cleaving to provide a plurality of cleaved device layers, and bonding the cleaved device layers together to form the multi-layered storage structure.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a silicon wafer with implanted and deposited devices, according to an embodiment of the invention.

Figure 2 is a cross-sectional view of the Figure 1 wafer with a layer cleaved therefrom, according to an embodiment of the invention.

Figure 3 is a cross-sectional view of the Figure 2 wafer and layer, with additional devices implanted and deposited on the wafer, according to an embodiment of the invention.

Figure 4 is a cross-sectional view of the Figure 1 wafer with a second layer cleaved therefrom, according to an embodiment of the invention.

Figure 5 is a cross-sectional view of the Figure 4 wafer and layers, with additional devices implanted and deposited on the wafer, according to an embodiment of the invention.

Figure 6 is a cross-sectional view of the Figure 1 wafer with a third layer cleaved therefrom, according to an embodiment of the invention.

Figure 7 is a cross-sectional view of three cleaved wafer layers bonded together, according to an embodiment of the invention.

Figure 8 is a cross-sectional view of a cleaved wafer applied to conductive traces, according to an embodiment of the invention.

Figure 9 is a cross-sectional view of diode pillars formed on conductive traces, according to an embodiment of the invention.

Figure 10 is a cross-sectional view of a metal layer applied to the Figure 9 structure, according to an embodiment of the invention.

Figure 11 is a cross-sectional view of a cross-point array formed from the Figure 10 structure, according to an embodiment of the invention.

Detailed Description

A method of making a multi-layered memory or other electronic storage structure according to an embodiment of the invention includes forming device layer 10 on single-crystal silicon wafer 15, as shown in Figure 1. Device layer 10 includes devices such as diodes, transistors, antifuses, tunnel junctions, etc.,

which are implanted, deposited, or otherwise formed or provided in layer 10. Other examples of such devices include, but are not limited to, charge-coupled devices (CCDs), complementary metal oxide semiconductor (CMOS) imagers and other CMOS devices, tunnel diodes, charge pumps, and other devices.

As shown in Figure 2, the method further includes cleaving device layer 10 from wafer 15. Cleaved portion 20 includes device layer 10 and cleaved wafer section 25. Ion-implantation induced layer splitting of wafer 15, for example, using hydrogen or other light species, accomplishes the cleaving of portion 20 from wafer 15. The hydrogen or other ion penetrates to a desired depth and causes weakening at that depth upon heating. The weakening of the silicon layer causes cleaved wafer section 25 and device layer 10 to split or "peel" off wafer 15, allowing layer transfer to occur. According to another example, a layer of porous silicon is formed by anodic etching and annealing, to form the splitting layer. Other methods of cleaving portion 20 from wafer 15 also are contemplated.

As shown in Figure 3, additional device layer 30 then is formed on wafer 15. As shown in Figure 4, layer 30 and an associated cleaved wafer section 35 together form cleaved wafer portion 40, which is cleaved from wafer 15 in the same manner as cleaved wafer portion 20. The method thus includes repeating the forming and cleaving to provide a plurality of cleaved device layers originating from the same single-crystal silicon wafer 15. Figures 5-6 illustrate an additional repetition of the forming and cleaving, with additional device layer 50 and associated cleaved wafer section 55 forming another cleaved wafer portion 60.

The method also includes, as shown in Figure 7, bonding the cleaved device layers 10, 30, 50 together, along with their associated cleaved wafer sections 25, 35, 55. Alternatively, parts or all of sections 25, 35, 55 optionally are removed or altered, for example by chemical mechanical polishing or planarization (CMP), to planarize the surface thereof and/or to define a metal interconnect pattern before bonding. The bonding optionally is accomplished using plasma-activated bonding, a similar silicon-on-insulator (SOI) process, or other standard bonding or laminating processes. Bonded wafer portions 20, 40,

60 together form multi-layered electronic storage structure 70, for example flash memory or other memory, a cross-point memory or other cross-point structure, one or more processors, etc. Structure 70 thus is a memory stack, for example, comprising a plurality of bonded memory layers 20, 40, 60 or 10, 30, 50, each memory layer being cleaved from single-crystal silicon wafer 15. Structure 70 optionally is used in forming a three-dimensional cross-point array memory structure.

Figures 8-11 illustrate a cross-point array structure having crystalline isolated diode pillars, using one or more cleaved wafers, and a method of making such a structure. Cleaved wafer portion 100 is provided from a wafer, such as wafer 15, in the manner described earlier. According to one example, wafer portion 100 is uniformly N-doped and/or forms N and P regions, as illustrated in Figure 8. Conductive traces, such as row lines 105 formed of metal or silicide, for example, are provided on a base substrate or wafer (not shown). Cleaved portion 100 is placed over and bonded to row lines 105. Cleaved portion 100 includes sacrificial wafer portion 110, which is removed by CMP or other process after bonding.

With reference to Figure 9, wafer portion 100 is lithographically etched to form vertical diodes 115. Viewed from the top, diodes 115 form a checkerboard pattern, according to one example. An interlayer dielectric (ILD) is applied, and a CMP process follows. Antiferromagnetic (AF) layer 120 then is applied, as shown in Figure 10. AF layer 120 is a stress-relieve-oxide (SRO) - type AF layer, according to one example, to provide thicker oxide and better manufacturing tolerance. Metal layer 125 then is deposited. Figure 10 also illustrates optional storage layer 130 applied between row lines 105 and diodes 115.

As shown in Figure 11, metal layer 125 then is etched to form columns or column lines 135. ILD 140 then is deposited. CMP, application of additional layers, and/or other processing then occurs to form a complete cross-point structure. An insulating dielectric layer optionally is applied above column lines 135, for example, and then one or more additional complete sets of row lines 105, diodes 115, column lines 135 and/or other components added to form a

stack of desired size, e.g. in the manner of layers or portions 20, 40, 60 of Figure 7. It should be noted that separate etching of diodes 115 as represented in Figure 9 can be eliminated, and column lines 135 instead used as a mask to create diodes 115 in Figure 11. In either case, the resulting cross-point structure includes row lines 105, crystalline isolated diode pillars 115 crossing row lines 105, pillars 115 being formed from a cleaved wafer as described, and column lines 135 crossing pillars 115 and row lines 105. Diode pillars 115 are together cleaved from e.g. wafer 15 in a layer or portion 100, which is applied above row lines 105. Diodes 115 are P-N diodes, as illustrated, but also optionally comprise Schottky diodes or PIN diodes if desired. Antiferromagnetic layer 120 is applied between diode pillars 115 and column lines 135, and optional storage layer 130 is applied between row lines 105 and diode pillars 115. The cross-point structure optionally comprises memory, such as magnetic memory or other nonvolatile memory.

According to additional embodiments, a method of making a cross-point array structure includes patterning and/or implanting a single-crystal silicon wafer such as wafer 15, for example, with a pattern of squares generally in the manner of a checkerboard. A layer, such as layer 100, is cleaved from the patterned wafer, and the cleaved layer is applied over conductive traces such as row lines 105. The cleaved layer optionally is a P-N layer or other layer, as mentioned previously. Layer 100 is etched to create vertical diodes 115 in communication with conductive traces 105. A second conductive layer 125 is applied over layer 100, and conductive traces such as column lines 135 are patterned therefrom. Column lines 135 optionally are used in masking and patterning cleaved layer 100.

Embodiments of the invention provide performance advantages associated with single-crystal silicon, e.g. for devices in the upper levels of the cross-point or other array or structure. Embodiments of the invention are used to produce memory, such as flash memory or other nonvolatile memory with ability to block erasure of stored information. Such nonvolatile memory is competitive in speed with dynamic RAM, or at least roughly comparable, and provides virtually instant-on capabilities even after a power-off condition.

Embodiments of the invention also provide high density, and high performance with dynamic switching. Other aspects of the invention will be apparent to those of ordinary skill.